REMARKS

Claims 1, 2, 4-9 are pending in this application. Claim 3 has been canceled and claim 9 has been newly added. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Claims have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. It is believed that this Amendment is fully responsive to the Office Action.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Specification

The disclosure has been objected to due to certain informalities, which the Examiner deemed needed correction.

As to the Examiner's outstanding objection to the Abstract of the Disclosure, the Applicant has deleted the current Abstract, and submit herewith a substitute Abstract of the Disclosure in place therefor.

Applicant respectfully requests that the substitute Abstract of the Disclosure submitted herewith be approved by the Examiner.

Also, applicant respectfully submits that the amendments to the specification obviate the objection to the specification. Accordingly, withdrawal of the objection to the specification is respectfully solicited.

Claim Objections

Claims 1-8 have been objected to because of informalities.

In response to the objections, the informalities have been corrected and the objections have been overcome.

Rejections under 35 USC §102(b)

Claims 1-4 and 5-8 stand rejected under 35 USC §102(b) as being anticipated by Cantell et al (U.S. Patent No. 6,255,179).

Applicant respectfully traverses this rejection.

Claim 1 has been amended to recited "wherein the wiring thinning step comprises the steps of: oxidizing the wiring, using a rapid thermal processing apparatus, beginning on an upper surface thereof down to a predetermined depth; and removing an oxidized section of the wiring oxidized in the oxidizing step." The recitation, "oxidizing the wiring, using a rapid thermal processing apparatus" is supported on page 7 of the present specification.

In Cantell et al a surface of the silicon wafer is reacted with a plasma source (see column 2, lines 23-24, and column 3, lines 55-61). Cantell et al does not teach or suggest the rapid thermal processing.

For at least this reason, claim 1 patentably distinguish over Cantell et al.

Thus, the 35 USC §102(b) rejection should be withdrawn.

New Claim

New claim 9 has been added. The subject matter of claim 1 is supported on page 7 in the present specification.

In view of the aforementioned amendments and accompanying remarks, claims , as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Sadao Kinashi

Sadao Kinashi
Attorney for Applicant
Reg. No. 48,075

SK/fs
Atty. Docket No. **011317**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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PATENT TRADEMARK OFFICE

Enclosures: Version with Markings to Show Changes Made
Substitute Abstract of the Disclosure

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VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/995,575

IN THE ABSTRACT:

The Abstract has been amended as follows:

A wiring of silicon is formed on a surface of a semiconductor substrate. Part of the wiring is covered with a resist pattern. Ion implantation is conducted on the substrate using the resist pattern as a mask and then the resist pattern is removed. An upper section of the wiring with a thickness of at least 5 nm is removed to minimize thickness of the wiring. Reaction is caused between a surface section of the thinned wiring ~~of which thickness is thus reduced~~ and a metal which reacts with silicon to form silicide to thereby form a metal silicide film on a surface of the wiring. Resistance of the wiring can be reduced with good reproducibility.

IN THE SPECIFICATION:

The paragraph at page 2, lines 13-23 has been amended as follows:

According to one aspect of the present invention, there is provided a method for manufacturing a semiconductor device, comprising the steps of: forming a wiring comprising silicon on a surface of a semiconductor substrate; covering part of the wiring with a resist pattern; implanting ions into the wiring using the resist pattern as a mask; removing the resist pattern; removing a surface layer of the wiring to a depth of at least 5 nm to thin the wiring; and forming a metal silicide film on a surface of the wiring by

causing reaction between a surface layer of the thinned wiring ~~of which thickness is thus reduced~~ and a refractory metal which reacts with silicon to form silicide.

The paragraph from page 2, line 24 to page 3, line 9 has been amended as follows:

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor device, comprising the steps of: forming wiring comprising silicon on a surface of a semiconductor substrate; covering part of the wiring with a resist pattern; implanting ions into the wiring using the resist pattern as a mask; removing the resist pattern; oxidizing the wiring beginning on an upper surface thereof ~~up~~ down to a predetermined depth ~~thereof~~; removing an oxidized section of the wiring oxidized in the oxidizing step and thereby thinning the wiring; and forming a metal silicide film on a surface of the wiring by causing reaction between a surface section of the thinned wiring ~~of which thickness is thus reduced~~ and a refractory metal which reacts with silicon to form silicide.

The paragraph at page 8, lines 11-21 has been amended as follows:

As shown in Fig. 2E, a cobalt silicide film 25 is formed on an upper surface of the wiring 3. Description will now be given of a method of forming the cobalt silicide film 25. A 10 nm thick cobalt (Co) film and a 30 nm thick ~~titan~~ titanium nitride (TiN) film are deposited on the overall surface of the silicon substrate 19 by sputtering. In a nitrogen gas atmosphere, thermal treatment is performed for 30 seconds at 500 °C. As a result of reaction between the wiring 3 and the cobalt film, a cobalt silicide film 25 is

formed. The cobalt film which did not react with the wiring 3 and the titan nitride film are removed in a wet process using a mixture including sulfuric acid and hydrogen peroxide.

IN THE CLAIMS:

Claim 3 has been canceled.

Claim 9 has been added.

Claims 1 and 5 have been amended as follows:

1. (Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming a wiring comprising silicon on a surface of a semiconductor substrate;

covering part of the wiring with a resist pattern;

implanting ions into the wiring using the resist pattern as a mask;

removing the resist pattern;

thinning the wiring by removing a surface layer of the wiring to a depth of at least 5 nm ~~to thin the wiring~~; and

forming a metal silicide film on a surface of the wiring by causing reaction between a surface layer of the thinned wiring ~~of which thickness is thus reduced~~ and a refractory metal which reacts with silicon to form silicide,

wherein the wiring thinning step comprises the steps of:

oxidizing the wiring, using a rapid thermal processing apparatus, beginning on an upper surface thereof down to a predetermined depth; and

removing an oxidized section of the wiring oxidized in the oxidizing step.

5. (Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming wiring comprising silicon on a surface of a semiconductor substrate;

covering part of the wiring with a resist pattern;

implanting ions into the wiring using the resist pattern as a mask;

removing the resist pattern;

oxidizing the wiring, using a rapid thermal processing apparatus, beginning on an upper surface thereof ~~up~~ down to a predetermined depth ~~thereof~~;

removing an oxidized section of the wiring oxidized in the oxidizing step and thereby thinning the wiring; and

forming a metal silicide film on a surface of the wiring by causing reaction between a surface section of the thinned wiring ~~of which thickness is thus reduced~~ and a refractory metal which reacts with silicon to form silicide.

ABSTRACT OF THE DISCLOSURE:

A wiring of silicon is formed on a surface of a semiconductor substrate. Part of the wiring is covered with a resist pattern. Ion implantation is conducted on the substrate using the resist pattern as a mask and then the resist pattern is removed. An upper section of the wiring with a thickness of at least 5 nm is removed to minimize thickness of the wiring. Reaction is caused between a surface section of the thinned wiring and a metal which reacts with silicon to form silicide to thereby form a metal silicide film on a surface of the wiring. Resistance of the wiring can be reduced with good reproducibility.